REMARKS

Applicant appreciates the detailed examination evidenced by the Office Action mailed February 13, 2006 (hereinafter "Office Action"). In response, Applicant has amended independent Claim 1 to incorporate the recitations of Claims 2 and 6, has amended independent Claim 16 to incorporate the recitations of Claims 17 and 20, and has amended independent Claim 30 to incorporate analogous method recitations along the lines of amended Claim 1. Independent Claim 35 has been amended to correct a typographical error. Claims 2, 6, 12, 17, 20, 26-29 and 31 have been canceled, and several of the dependent claims have been amended in keeping with the amendments to the independent claims and/or to correct typographical errors. Applicant respectfully submits that amended independent Claims 1, 16, and 30 are patentable over the combination of Applicant's Alleged Admitted Prior Art ("AAPA"), U.S. Patent No. 6,288,953 to Kwak ("Kwak") and U.S. Patent No. 6,757,212 to Hamamoto et al. ("Hamamoto") cited in rejecting Claims 6 and 20. Applicant traverses the rejection of independent Claim 35, because the cited combination of U.S. Patent No. 5,068,831 to Hoshi et al ("Hoshi") and U.S. Patent No. 6,192,003 to Ohta et al. ("Ohta") does not disclose or suggest all of the recitations of Claim 35, and because the Office Action fails to provide clear and particular evidence from the prior art of a motivation or suggestion to combine these references. Applicant further submits that several of the dependent claims have independent bases for patentability.

Amended Independent Claims 1, 16 and 30 are patentable

As amended, Claim 1 recites:

> A data path, comprising:
> a downstream stage that strobes data at an input thereof responsive to a first control signal;
> a first upstream stage that sends data to the input of the downstream stage responsive to a second control signal;
> a second upstream stage that sends data to an input of the first upstream stage responsive to a third control signal having a timing with respect to the second control signal that varies responsive to a frequency at which data is transferred along the data path; and
> a control circuit operative to selectively fix timing of the second control signal to one of timing of the first control signal and timing of the third control signal.

Amended independent Claims 16 and 30 include corresponding recitations. An example of such recitations is illustrated in FIGs. 6 and 7A-B and the description thereof at pages 7 and 8 of the present application.

In rejecting Claim 6, the Office Action cites Kwak as allegedly teaching "a data path wherein the control circuit is further operative to selectively fix timing of the second control signal to one of timing of the first control signal and timing of the third control signal (column 7[sic], line 27, through column 2, line 23). Office Action, p. 10. Applicant assumes that the Office Action means to cite column 1, line 27 through column 2, line 23, which describe Figs. 1-3 of Kwak.

Nowhere in this passage does Kwak disclose or suggest the selectively timing fixation recited in Claim 1. In particular, Fig. 1 of Kwak shows a data path including a sense amplifier 160 and a downstream data buffer 170. Fig. 2 shows an address transition detection circuit and sense amplifier control circuit that generates sense amplifier control signals SACS1-4 and a sense amplifier latch control signal SAC, while Fig. 3 is a timing diagram illustrating operation of the circuit of Fig. 2. It is unclear from the Office Action as to what in Kwak corresponds to the recited first, second and control signals of "selectively fix timing of the second control signal to one of timing of the first control signal and timing of the third control signal" recited in Claim 1 but, even if it is assumed that these signals are among the sense amplifier control signals SACS1-4 and a sense amplifier latch control signal SAC shown in Figs. 1-3 of Kwak, nowhere does it appears that timing of any one of these signals is ***selectively*** fixed to timing of one of two of the other signals. Rather, the sense amplifier control signals SACS1-4 and the sense amplifier latch control signal SAC have a static causal relationship, *e.g.*, the second sense amplifier control signal SACS2 follows from the first sense amplifier control signal SACS1, the third sense amplifier control signal SACS3 follows from the second sense amplifier control signal SACS2, etc., as shown in Fig. 3.

Accordingly, Kwak does not provide the teachings alleged in the Office Action, and the cited combination of AAPA, Kwak and Hamamoto does not teach or suggest all of the recitations of independent Claim 1, as amended. For at least these reasons, Applicant

submits that amended independent Claim 1 is patentable. At least similar reasons support the patentability of amended independent Claims 16 and 30.

Independent Claim 35 is patentable

Claim 35 recites:

> A method of characterizing a data path comprising a first driver-receiver pair including a first driver circuit and a first receiver circuit and a second driver-receiver pair comprising a second driver circuit and a second receiver circuit, the method comprising:
>
> fixing timing of an enable signal for the first driver circuit to timing of an enable signal for the first receiver circuit and fixing timing of an enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit ***while increasing a rate at which data is passed through the data path to determine a minimum delay between the second driver circuit and the second driver circuit***; and
>
> fixing timing of the enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit and fixing timing of the enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit ***while increasing a rate at which data is passed through the data path to determine a minimum delay between the first driver circuit and the first receiver circuit.***

An example of such operations is provided in the present application at pages 8 and 9 with reference to Figs. 7A-B, which describes a process whereby a series of driver/receiver pairs may be characterized in a sequential manner.

In rejecting Claim 35, the Office Action alleges that Hoshi discloses the first and second driver circuits, the first and second receiver circuits, and "data rate can be increased or decreased and timing issues can be altered via control circuits (equalization circuits 41 and 42)". Office Action, p. 6. The Office Action concedes that Hoshi does not disclose:

> . . . controlling an enable signal for the first driver circuit to timing of an enable signal for the first receiver circuit and controlling an enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit; and controlling an enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit and controlling an enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit . . ,"

but asserts that such missing teachings are provided by Ohta, which shows "a timing control circuit (21) is responsive for delaying various control signals . . . in a cascading manner via delay circuits (as shown in figure 2) dependent on the previous signal." Office Action p. 7.

Respectfully, this is not what is claimed in Claim 35, and the alleged motivation provided for this combination of Hoshi and Ohta does not meet the requirements for combining references under 35 U.S.C. § 103.

Claim 35 describes particular operations that are performed under respective different sets of constraints on the timing of the various enable signals "to determine a minimum delay between the second driver circuit and the second receiver circuit" and "to determine a minimum delay between the first driver circuit and the first receiver circuit." There is nothing in Hoshi and/or Ohta that corresponds to this. In particular, the cited Fig. 12 of Hoshi merely shows a series combination of sense amplifiers wherein complementary data lines are equalized (i.e., charged to the same voltage) prior to sensing operations, while the cited material from Ohta merely describes generation of sense amplifier enable, bit line precharge, row decoder enable, column address latch signals, etc. There is nothing in Ohta corresponding to the selective control of enable signals of driver/receiver pairs as recited in Claim 35. Moreover, the stated basis for combining Hoshi and Ohta, i.e., "having a latency of 1 clock cycle" appears to be irrelevant to the operations recited in Claim 35, and provides no evidence as to how a ***combination*** of Hoshi and Ohta might be made or why such a combination would be effective; for example, the Office Action fails to specifically indicate how the cited control circuit from Ohta could be used with the circuitry shown in Hoshi. Accordingly, Applicant submits that the cited combination of Hoshi and Ohta does not disclose or suggest all of the recitations of Claim 35, and that there is insufficient evidence from the prior art of a motivation or suggestion to combine Hoshi and Ohta. For at least these reasons, Applicant submits that Claim 35 is patentable.

The dependent claims are patentable

Applicant submits that dependent Claims 3-5, 7-11, 13-15, 18, 19, 21-25, 32-34 and 36-39 are patentable at least by virtue of the patentability of the various ones of independent Claims 1, 16, 30 and 35 from which they depend. Applicant further submits that several of these dependent claims are separately patentable.

For example, Claim 5, which stands rejected as obvious over AAPA, Kwak and Hamamoto, recites " wherein the fixed delay circuit comprises a fixed delay circuit in a forward path of a delay locked loop (DLL) or a phase locked loop (PLL)." In rejecting Claim

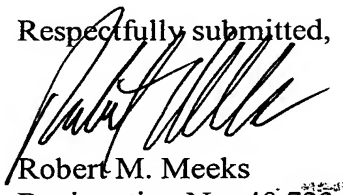
5, the Office Action asserts that Hamamoto discloses such recitations at column 42, lines 14-30. See Office Action, p. 10. Applicants submit that this is incorrect. The cited passage states that the "phase-adjusted clock signal LCLK . . . is adjusted in phase relative to an external clock signal and has a delay time (fixed delay) which is not dependent on the clock frequency" and Fig. 36 includes a vague labeling "FIXED DELAY (DLL/PLL)," but these portions of Hamamoto clearly do not disclose or suggest "a fixed delay circuit ***in a forward path of*** a delay locked loop (DLL) or a phase locked loop (PLL)." Accordingly, the cited combination of references does not disclose or suggest all of the recitations of Claim 5 and, for at least these reasons, Applicant submits that Claim 5 is separately patentable. At least similar arguments support the separate patentability of Claim 19.

Claim 11, which stands rejected as obvious over a combination of AAPA, Kwak, Hamamoto and Ohta, recites "wherein the control circuit is further operative to selectively fix timing of the fourth control signal to one of timing of the third control signal and timing of the fifth control signal." As noted above with reference to Claims 1, 16, and 30, AAPA, Kwak and Hamamoto do not disclose such selective timing fixation. The portions of Ohta cited at page 15 of the Office Action also fail to provide such teachings. In particular, the Office Action alleges that row address latch 14 and row decoder 13 shown in Fig. 1 of Ohta are stages in a data path. This is clearly erroneous, as the row decoder 13 does not convey data anywhere, but instead selects word lines WL of a memory cell array 11. Accordingly, Ohta does not provide the teachings alleged in the Office Action and, for at least these reasons, Applicant submits that Claim 11 is separately patentable. Applicant submits that Claim 25 is separately patentable for at least similar reasons.

CONCLUSION

Applicant submits that all of the claims are now in condition for allowance for at least the foregoing reasons. Applicant respectfully requests allowance of the claims and passing of the application to issue in due course. Applicants urge the Examiner to contact Applicant's undersigned representative at (919) 854-1400 to resolve any remaining formal issues.

Respectfully submitted,



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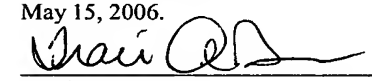

Traci A. Brown